2009

Nano-switch for Study of Gold Contact Behavior

Adam Fruehling
Purdue University - Main Campus, soimems@purdue.edu

Shijun Xiao
Purdue University - Main Campus

Minghao Qi
Birck Nanotechnology Center, Purdue University, mqi@purdue.edu

Kaushik Roy
Purdue Univ, Sch Elect & Comp Engn, Network Computat Nanotechnol, kaushik@purdue.edu

Dimitrios Peroulis
Birck Nanotechnology Center and School of Electrical and Computer Engineering, Purdue University, dperouli@purdue.edu

Nano-switch for Study of Gold Contact Behavior

Adam Fruehling, Shijun Xiao, Minghao Qi, Kaushik Roy, Dimitrios Peroulis
School of Electrical and Computer Engineering, Purdue University
Birck Nanotechnology Center
West Lafayette, IN 47907
Email: fruehlin@purdue.edu, sxiao@purdue.edu, mqi@purdue.edu, kaushik@ecn.purdue.edu, dperouli@purdue.edu

***Abstract*— In this paper we present the fabrication and characterization of a new NEMS DC switch as a vehicle to characterize Au-to-Au contacts at nano-scale. The switch consists of a 1050-nm long, 200-nm wide and 50-nm thick cantilever gold beam. The measured on-state resistance values range from 83 Ω to 640 Ω and the actuation voltages from 4 V to 22 V. All measurements are conducted at a current of 1 μA and the obtained values are in good qualitative agreement with traditional elastic-plastic contact models. The calculated switching time is 55 ns. Characterization of contacts at nano-scale will be critical for the success of NEMS devices used in ultra low-power sensors. To this end, we examine the impact of such a switch as a leakage control mechanism.**

I. Introduction

The ongoing demand for high-performance low power sensor electronics has placed a significant focus on increasing the available computing power for a given battery life. Miniaturization of such components has lead to dramatic increases in leakage current. This has become a serious inhibiting factor in achieving low-power electronics [1]. Similarly, in high performance computing, subthreshold leakage has been a major hindrance to technology scaling. Furthermore, technology scaling is also rendering many well-known techniques such as sleep transistor insertion [2], dual/multi V_{th} design, multi V_{DD} [3], selective clock gating [2], reverse body biasing (RBB) [4] etc., inefficient. In contrast to these solid-state implementations, there is no leakage current for MEMS [5] or NEMS even when dimensions are reduced.

Switches of comparable dimensions [6] to those presented here offer great potential in realizing ultra low-power digital memory circuits [7], sensors [8], or as a leakage control circuit. Despite the growing interest around 2 and 3-terminal carbon nanotube devices, more traditional NEMS fabrication techniques offer an important practical avenue for the investigation of contact metal behavior at nano-scale. We demonstrate the feasibility of NEMS for this approach by successfully implementing and testing a nanomechanical switch that is 1050-nm long, 200-nm wide and 50-nm thick. Besides an infinite off-state resistance that guarantees zero leakage, the switch exhibits a measured on-state resistance as low as 83 Ω, a measured current handling ability of > 1 μA, and a calculated switching time of 55 ns.

We also show that integrating this type of switch as a mechanical-sleep transistor in a variety of VLSI circuits would dramatically reduce their leakage, while at the same time affect their response time by only 0.5 to 10% depending on the circuit complexity. Although reliability of NEMS switches is still an open question in the literature, this study shows for the first time a significant application space of NEMS devices that may result in significant power savings.

II. Device Details

A representative NEMS switch is shown in Figure 1 in its up (off) state. The switch was fabricated on a thermally

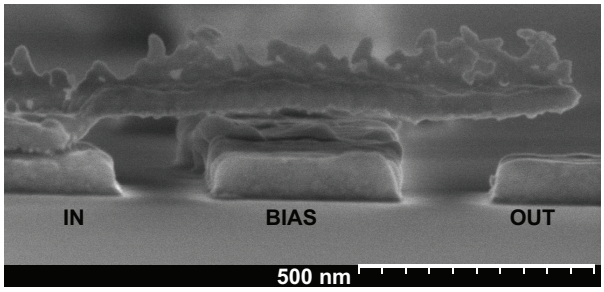

Fig. 1. 10 kV SEM image of switch in up (off) position.

oxidized silicon wafer utilizing lift-off techniques with a bi-layer resist. Patterning was achieved using the Vistec VB6 E-beam lithography system at Purdue University. The complete fabrication process is shown in Figure 2 and is summarized as follows:

(a) Spin PMMA on oxidized wafer and perform e-beam exposure
(b) Develop PMMA and evaporate gold
(c) Lift-off resist and gold
(d) Spin PMMA and Copolymer
(e) High-dose aligned e-beam exposure for PMMA
(f) Low-dose aligned e-beam exposure for copolymer
(g) Develop resist
(h) Evaporate gold
(i) Lift-off resist and gold, release, and critical-point dry.

Table II provides a summary of designed device dimensions and calculated switch parameters.

III. Contact Investigation

The fabricated switches were tested with the setup shown in Figure 3. Contact resistance and actuation voltage were experimentally determined at a 1 μA input current. Switch contact resistance was measured to be between 640 Ω and decreased to 83 Ω with increasing contact force as expected. The corresponding biasing voltages range from 4 to 22 V. We also compared the measured contact resistance with the values

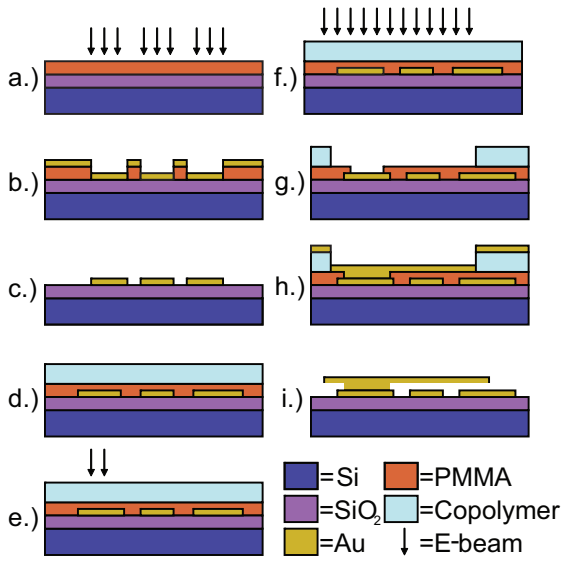

Fig. 2. Fabrication Process

TABLE I

Basic Switch Parameters

Observed Parameters	
Length [nm]	1050
Width [nm]	200
Thickness [nm]	50
Off Bias Gap [nm]	100
On Bias Gap [nm]	50
Calculated Parameters	
Spring Constant [N/m]	0.46
Au Young's Modulus [GPa]	86
Poisson's Ratio	0.44
Pull-in Voltage [V]	14.5
Switching Time [ns]	55
Au Mean Free Path [nm]	38
Crit. vert. asperity deformation α_c (pm)	105

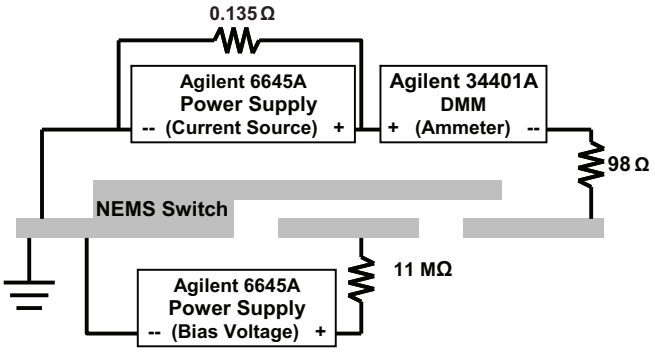

Fig. 3. Test setup for determining actuation voltage and contact resistance.

predicted by the elastic-plastic model of deformation [10]. Due to the fabrication process, the bottom surface of the switch is significantly rougher than the top surface of the output electrode. As a result, the latter surface is assumed smooth. Based on the switch SEM images, we deduce an average contact radius of curvature of 85 nm. The electrostatically induced contact force ranges from 2.3 to 69 nN for the specified applied biases. Due to the switch size and this relatively weak contact force we assume that only one asperity is in contact at the down state. Displacement and contact resistance calculations typically require more complicated models than the ones employed for MEMS switches [9]. However, assuming the models employed by [9] and [10] apply here, the vertical deformation of the contacting asperity ranges from 23 to 221 pm for applied voltages from 4 to 22 V respectively. The calculated critical asperity radius is 105 pm [10]. Thus the contact is fully elastic for voltages below 12.6 V and it enters the elastic-plastic region for higher voltages as this deformation thresholds value is exceeded. Based on these results, the contact resistance can be calculated to be between 15 and 209 Ω. Table II summarizes all the model parameters. It is interesting to note that, unlike MEMS switches, the Knudsen number for the contact (mean free electron path over contact radius) is greater than about 10 and therefore the contact resistance is dominated by ballistic transport. Though measured resistance values are approximately 4 to 5 times higher than the calculated values, this is attributed to the environment around the switch (typical laboratory environment) that does not restrict contaminants away from the switch. However, it is worth noting that material properties may also deviate at this scale from the bulk values assumed for the calculations. Nevertheless, the model is physically meaningful and follows experimentally observed trends.

TABLE II

Basic Contact Parameters

V_a [a] [V]	4	13	20	22
$R_{c,meas}$ [b] [Ω]	640	144	109	83
$R_{c,calc.}$ [c] [Ω]	209	45	18	15
$R_{c,B}$ [d] [Ω]	203	41	16	14
α [e] [pm]	23	110	190	221
$r_{cont.}$ [f] [nm]	1.39	3.05	4.07	4.34
Knudsen #	27	12	8	7
Contact type	elastic	elastic -plastic	elastic -plastic	elastic -plastic

[a] *Actuation voltage*
[b] *Measured contact resistance*
[c] *Calculated contact resistance*
[d] *Calculated ballistic transport resistance*
[e] *Contact asperity vertical deformation. The contact type changes from elastic to elastic-plastic if this value exceeds the critical vertical deformation* $\alpha_c = 105$ *pm.*
[f] *Contact area radius*

IV. NEMS Switches as a Leakage Control Device

Leakage current during the sleep state presents a significant challenge to achieving ultra low-power sensors. Figure 5 schematically illustrates the proposed system-level concept with the nanomechanical switches. Their main advantages include zero off-state leakage (independent of scaling) and zero static power consumption in both states. A number of requirements, however, need to be met before this approach gains commercial potential including: a) reasonably low on-state resistance with low actuation voltage; b) adequate relia-

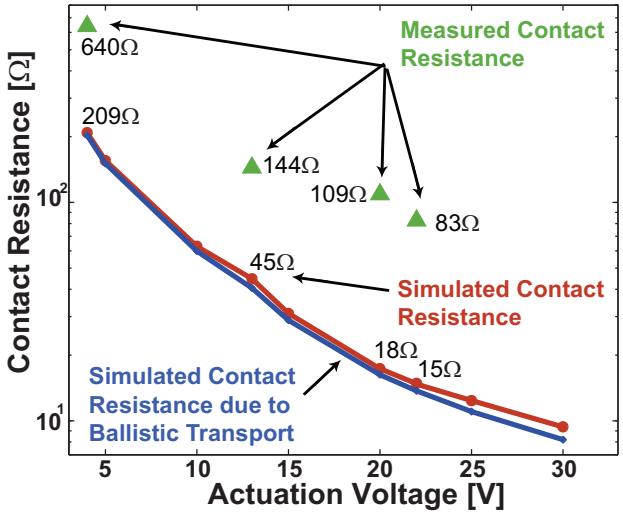

Fig. 4. Measured and simulated contact resistance values as a function of actuation voltage.

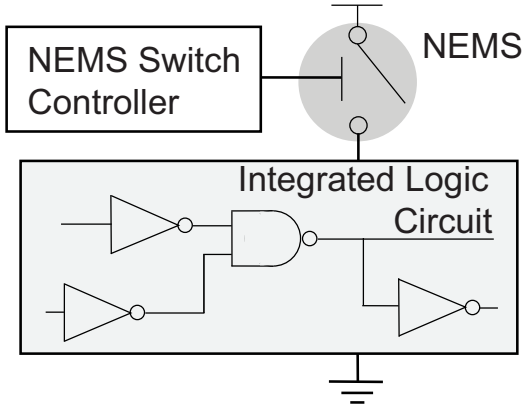

Fig. 5. Main concept for nanomechanical sleep transistor in low power sensor circuitry.

bility for a given application; and c) new power management schemes that consider the granularity level (number of controlled transistors per NEMS switch) and the NEMS switching frequency. This paper provides answers for the first question with a switch implementation that has the potential to satisfy all three requirements.

NEMS switches are not expected to match the reliability or manufacturing yield of solid-state transistors in the near future. Therefore, a meaningful integration scheme should be employed. The proposed implementation favors integration of NEMS leakage control switches at the circuit level as shown in Figure 5. To evaluate the effect of the NEMS switch on-state contact resistance we simulated the switching delay of several CMOS circuits of increasing complexity. As Figure 6 shows, the contact resistance of this NEMS switch is sufficiently low for all these circuits and it only reduces their speed by less than 0.5 to 10%. More complex circuits with tighter resistance requirements may require parallel connection of a few NEMS switches to meet performance criteria.

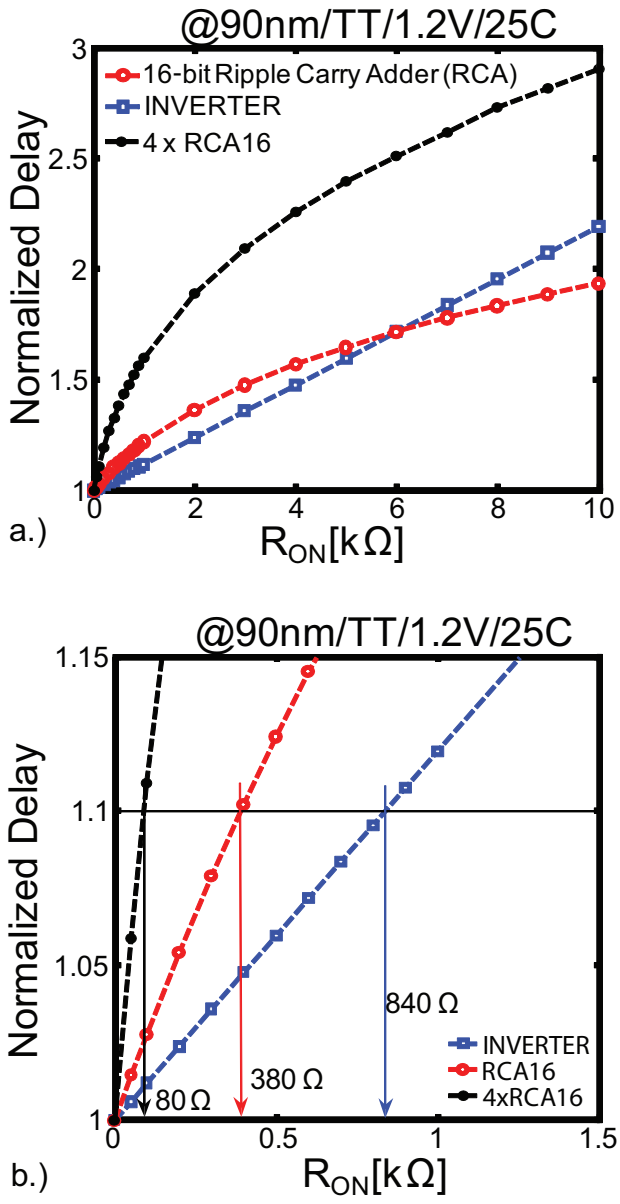

Fig. 6. (a.) Effect of R_{ON} of NEMS switch on normalized circuit delay (b.) Zoomed view of *(a)* with R_{ON} values corresponding to a delay penalty of 10% indicated

V. Conclusion

A device suitable for investigation of nano-scale behavior of metal contact interactions has been successfully fabricated and measured. Contact characteristics have been modeled and measured with good correlation to experimentally measured values, though further investigation is warrented into the study of metal contact material properties at nano scale. These devices represent a step forward in understanding the impact of device scaling on micro and nano electromechanical structures. Additionally, switches with suitable dimensions, current handling, and switching times for integration with power management circuitry for VLSI circuits with a minimal performance penalty have been fabricated and tested.

By choosing an appropriate implementation granularity level and using multiple NEMS in parallel, reliability and contact resistance can be achieved to meet performance demands required for further integration into ultra low-power sensor circuits.

REFERENCES

[1] K. Roy, S. Mukhopadhyay, H. Mahmoodi-Meimand, Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicron CMOS Circuits, IEEE Proceedings, vol. 91, pp. 305-327, February 2003.

[2] Z. Liu, C. Hu, J.-H. Huang, T.-Y. Chan, M.-C. Jeng, P.K. Ko, Y.C. Cheng, "Threshold voltage model for deep-submicrometer MOSFET's", *IEEE Trans. On Elec. Dev.*, vol 40, pp. 86-95, Jan. 1993

[3] R. Pierret, Advanced Semiconductor Fundamentals, Volume VI in Modular Series on Solid States Devices *Addison-Wesley Publishing Company*, 1989.

[4] F. Hamzaoglu, and M. Stan, "Circuit-Level Techniques To Control Gate Leakage For Sub-100 nm CMOS," *in Proceedings of ISLPED*, pp. 60-63, August 2002.

[5] A. Fruehling, K. Hagner, K. Roy, D. Peroulis, "RF MEMS Switches for Leakage Control in Wireless Handheld Devices" *Antennas and Propagation Symposium 2007*, pp. 97-100, June 2007

[6] Y. Tarakanov, J. Kinaret, A Carbon Nanotube Field Effect Transistor with a Suspended Nanotube Gate,*Nano Letters*, Vol. 7, pp. 2291-2294, Jun. 2007

[7] R. Blick et al., A nanomechanical computer exploring new avenues of computing, *New Journal of Physics*, Vol. 9 No. 7, Feb. 2007

[8] F. Albano et al., Design of an implantable power supply for an intraocular sensor using POWER, *Journal of Power Sources*, Vol. 170, pp. 216-224, Jun. 2007

[9] Jensen et. al., "Effect of Nanoscale Heating on Electrical Transport in RF MEMS Switch Contacts" *Journal of Microelectromechanical Systems*, vol. 14, No. 5, pp. 934-946, Oct. 2005

[10] R. Coutu et. al., "Micro-Switches with Sputtered Au, AuPd, Au-on-AuPt, and AuPtCu Alloy Electric Contacts", *IEEE Trans. Components Packaging Tech.*, vol. 29, No. 2, pp. 341-349, Jun. 2006